Hybrid Integrated Circuit

HSTR28S5R2

HSTR28S5R2F Specification for

Transient protection DC/DC Converter

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Specification for Transient Protection DC/DC Converter

1 Range

This specification specifies the HSTR28S5R2 and HSTR28S5R2F transient protection DC/DC converters for thick-film hybrid integrated circuit (Hereinafter referred to as the circuit).

2 Requirements

2.1 Design, construction and overall dimension

2.1.1 Process Structure

The circuit is manufactured by thick film hybrid integration process, bare chip assembly and metal hermetic package.

2.2.2 Absolute maximum rating

Input voltage V_I……80V

Output power P_o……32.5W

The storage temperature T_{stg}……-65℃～150℃

Lead resistance to soldering temperature (10s) T_h ……300℃

Junction temperature T_j……175℃

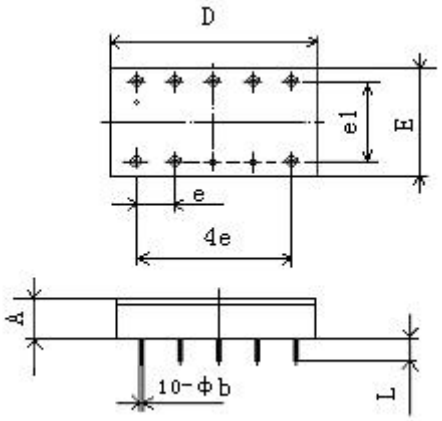
2.2.3 Recommended Operating Condition

Input voltage V_I……15V～50V

The operating temperature range T_C……-55℃～125℃

2.2.4 Package Outline

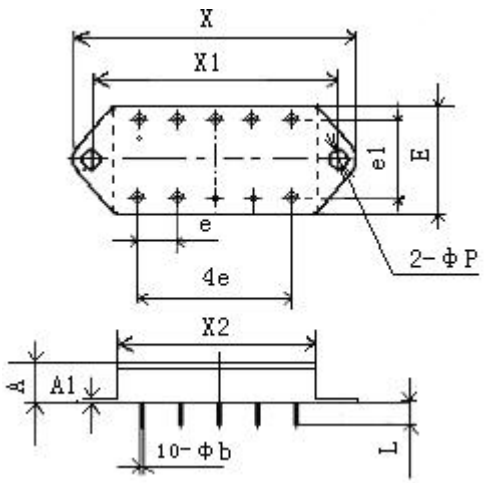
The circuit in a fully-sealed metal package, the model No. of the package is: UPP5429-10j (without flange), UPP5429-10n (with flange), and the outline and dimension of the package shall be as specified in Figure 1.



Unit: mm

Dimension Symbol	Data		
	Minimal	Nominal	Max.
A	-	-	10.66
φb	0.87	-	1.13
e	-	10．16	-
e1	-	20．32	-
D	-	-	54.40
E	-	-	29.00
L	5.40	-	-
Note: e and E1 refer to the interchangeability dimension, which is guaranteed by the manufacture and inspection of the package. There is no examination requirement in this specification.			

Figure 1a　HSTR28S5R2 Dimension



Unit: mm

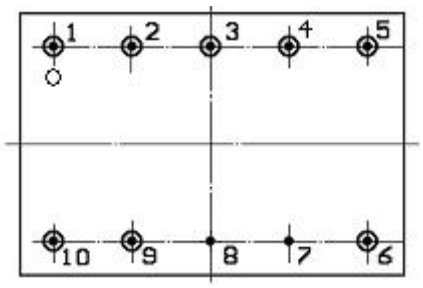
Dimension Symbol	Data

	Minimal	Nominal	Max.
A	-	-	10.66
A1	1.20	-	1.80
ϕb	0.87	-	1.13
e	-	10．16	-
e1	-	20．32	-
E	-	-	29.00
L	5.40	-	-
ϕP	3.80	-	4.40
X	-	-	74.00
X1	64.27	-	65.27
X2	-	-	54.40
Note: e and E1 refer to the interchangeability dimension, which is guaranteed by the manufacture and inspection of the package. There is no examination requirement in this specification.			

Figure 1b　HSTR28S5R2F Outline Dimension

2.2.5 Leading-end Arrangement

The arrangement of the terminal shall be as specified in Figure 2.



(Bottom view)

Outlet Sequence Number	Symbol	Function	Outlet Sequence Number	Symbol	Function
1	V_I	Input positive terminal	6	Sense+	Output positive sensing terminal
2	INH	Forbidden End	7	GND_C	Crustally

3	Sense-	Output Negative Sensing Terminal	8	GND_C	Crustally
4	GND_O	Outputly	9	SYN	Synchronous End
5	V_0	Output positive terminal	10	GND_I	Input ground

Fig. 2 Pin-out arrangement and Pin function

2.3 Electrical characteristic

Electrical characteristics shall be as specified in Table 1.

Table 1 Electrical characteristic

Characteristic	Symbol	Condition (Unless otherwise specify, *−55℃≤TC≤125℃ VI＝28V±0.5V,no external synchronization, C_L=0*）	A-group	Limit Value		Unit
				Minimal	Max.	
Output Voltage	V_0	Full load	1	5.14	5.26	V
			2，3	5.07	5.33	V
Output current	I_0	*VI=15V～50V*	1,2,3	-	6000	mA
Output ripple voltage (Peak-to-peak)	V_{RIP}	BW = 6MHz, full load	1,2,3	-	50	mV
Voltage regulation degree	S_V	*VI = 15V → 50V, full load*	1,2,3	-	20	mV
Current Regulation Degree	S_I	*IO = 0 → Full Load (6.0a)*	1,2,3	-	50	mV
Input current	I_I	No load, disable terminal connected to input ground	1,2,3	-	6	mA
		No load, no end open circuit	1,2,3	-	60	mA
Input Ripple Current (Peak-to-Peak)	I_{RIP}	BW = 20MHz, full load	1,2,3	-	50	mA
Efficiency	η	Full load	1,2,3	72	-	%
Insulation Resistance	R_I	Add 500V between input and output or between any terminal (except terminals 7 and 8) and housing, TA = 25 ℃	1	100	-	MΩ
Short-circuit protection function		Reduced-flow type protection	1,2,3	Have		

Capacitive load ab	C_L	*TA = 25 ℃, full load*	4	-	1000	μF
Switching frequency B	f_s	Full load	4,5,6	400	550	kHz
Output Voltage Change at Load Transient BC (Peak)	V_{LT}	50% load → Full load or Full load → 50% load	4,5,6	-500	500	mV
Recovery time of output voltage during load transients BCD	t_{LT}	50% load → Full load or Full load → 50% load	4,5,6	-	500	μs
Output Voltage Change (Peak) during Input Voltage Transient be	V_{VT}	Input voltage VI: 16 → 40V, full load Input voltage VI: 40 → 16V, full load	4,5,6	-600	600	mV
Output voltage recovery time bde during input voltage transient	t_{VT}	Input voltage VI: 16 → 40V, full load Input voltage VI: 40 → 16V, full load	4,5,6	-	500	μs
Startup Overshoot (Peak)	V_{T0}	Input voltage VI: 0 → 28V, full load	4,5,6	-	50	mV
Startup Delay f	t_d	Input voltage VI: 0 → 28V, full load	4,5,6	-	20	ms

- *The capacitive load can be anywhere from 0 to the maximum limit and has no effect on the DC parameters;*
- *This parameter is guaranteed by the design and is tested only during qualification inspections and design or process changes;*
- *The load jump time shall be greater than 10μs;*
- *Recovery time refers to the time from the start of the transition until the output voltage returns to the range of ± 1% of the corresponding stable value;*
- *The jump time of the input voltage shall be greater than 50us;*
- *The f-start delay time can be calculated either from the transition of the power supply or from the disconnection of the grounded inhibit terminal.*

2.4 Electrical Test Requirements

The electrical test requirements of the circuit shall be the relevant subgroups specified in Table 2, and the test of each subgroup shall be carried out as specified in Table 1 of this specification.

Table 2 Electrical test requirement

Test Requirement	Group
Intermediate electric test (before aging)	A1，A4
Final electrical test (after aging)	A1a，A2，A3，A4，A5，A6
Group a Inspection Requirements	A1，A2，A3，A4，A5，A6
Group C endpoint electrical test	A1

*This group calculate PDA.

2.5 Circuit Model

The circuit types are as follows: