Hybrid Integrated Circuit HDCD/ (20-50) -12-60/SP

Detail specification for radiation hardened DC/DC converters

1 Range

This specification specifies the detailed requirements for the design, production, screening, appraisal, certification, quality consistency inspection of the manufacturer of the hybrid integrated circuit HDCD/ (20-50) -12-60/SP radiation-resistant DC/DC converter (hereinafter referred to as the device) for aerospace use, as well as the quality assurance of the user's procurement, supervision and acceptance.

2 Requirements

2.1 Design, construction and dimensions

2.1.1 Absolute maximum ratings

A) Output power (PO);

B) The input voltage (VI) . 0 ~ 60V;

C) OpetemperTC:: ~ 1;

D) Storage temperature range (Tstg) -65 ℃ ~ 150 ℃;

E) The lead wire is resistant to soldering temperature (Th).

Note: Two or more absolute maximum rating conditions cannot be applied to the device at the same time.

2.1.2 Recommended working conditions

A) Input voltage (VI) . 20V ~ 50V;

B) OpetemperTC:: -~ 1;

C) Output current (IO)

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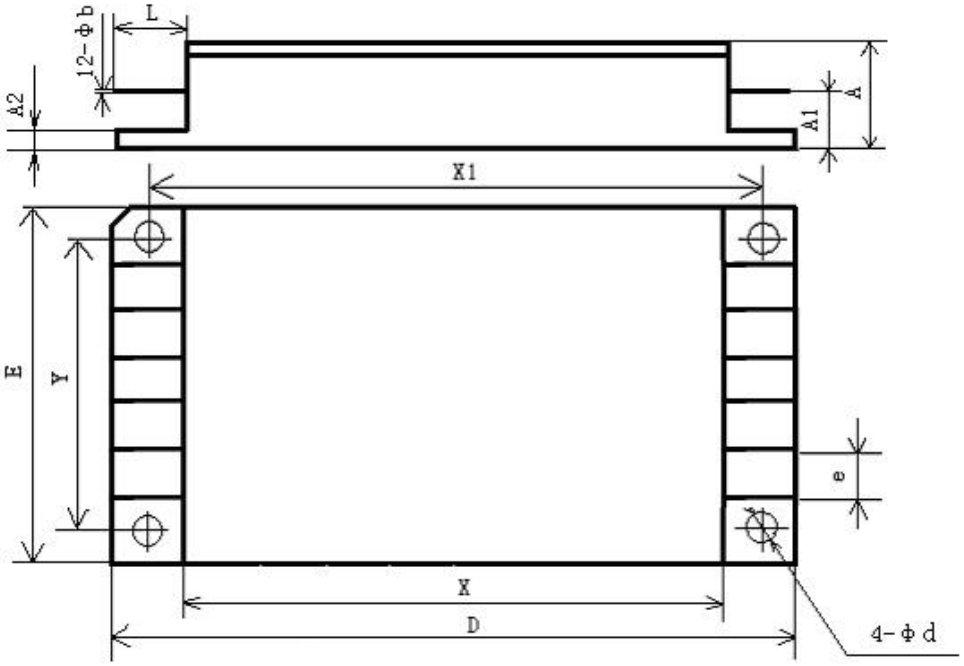
2.1.3 Package form

Package type: parallel seam welding;Shell shape: Metal flat shell.The external dimensions of the housing are specified in Figure 1.



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In Millimeters

Dimension Symbol	Numerical Value		
	Minimal	Nominal	Maximal
A	–	–	10.16
A1	5.29	–	5.89
A2	1.07	–	1.47
ϕb	0.87	–	1.13
ϕd	3.10	–	3.50
D	–	–	76.70
E	–	–	38.60
e	–	5.08	–
L	4.85	–	–
X	–	–	64.00
X1	69.90	–	70.30
Y	31.70	–	32.30
Note: e is the interchangeability dimension, which is guaranteed by the manufacturing and inspection of the shell, and is not required for examination in this specification.			

Fig. 1 Outline Dimension

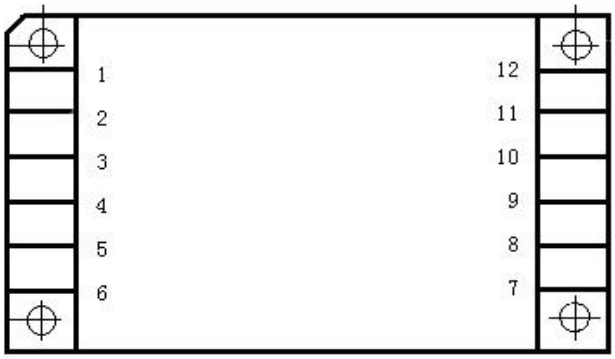
2.1.4 Lead materials and coatings

The outer lead-out end: the material is E type, the thickness of gold plating is 1.3 μm ~ 5.7 μm;

The cold-rolled steel shell circuit: the cover plate is plated with nickel, and the outer shell is plated with gold with the thickness not less than 1.0μm;

2.1.5 Outlet alignment and function

The arrangement of the leads shall be as specified in Figure 2.



Outlet serial number	Symbol	Function	Outlet serial number	Symbol	Function
1	VI	Input positive terminal	7	VO	Output Positive Terminal
2	GNDI	Input Ground Terminal	8	GNDO	Output Ground Terminal
3	NC	Null end	9	Sense-	Negative inductive end
4	INH1	Prohibited End 1	10	Sense+	Positive Induction End
5	SYNCOUT	Synchronous Output Terminal	11	SHARE	Current Sharing End
6	SYNCIN	Synchronous	12	INH2	Prohibited End

		Input			2

Fig. 2 Outlet Arrangement

2.1.6 Functional Block Diagram

The functional block diagram should conform to Figure 3.

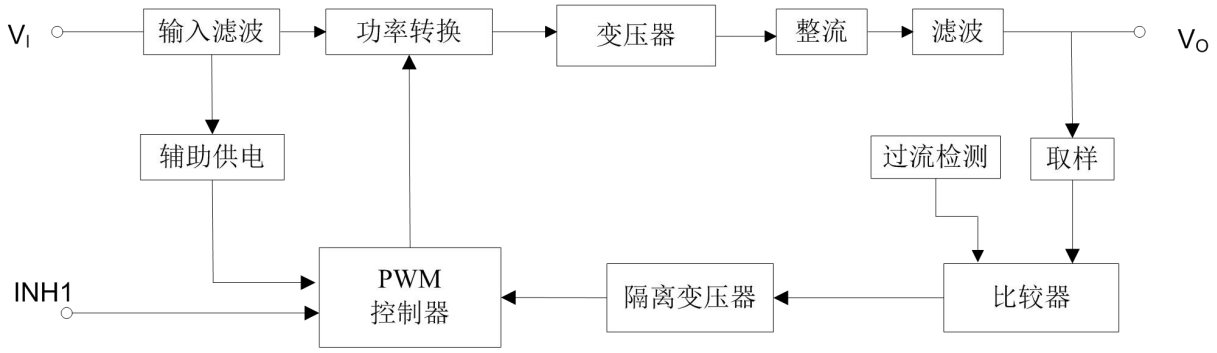


Figure 3. Functional Block Diagram

2.2 Weight

The total weight of the device does not exceed 95g.

2.3 Electrical characteristics

Unless otherwise specified, electrical characteristics shall be as specified in Table 1 and shall be applicable over the full temperature range.

Table 1 Electrical Characteristics

Preface Numb	Specific Property	Symbol	Condition (Unless otherwise specified, -55 ℃ ≤ TC ≤ 125 ℃ *VI = 28V ± 0.5V and VI = 42V ± 0.5V, forbidden open circuit, CL = 0)*	A-group Grouping	Limiting value		Unit
					Minimal	Maximal	

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er							
1	Output Voltage	*VO*	*IO=5A*	1	11.88	12.12	V
				2,3	11.76	12.24	
2	Output Current	*IO*	*VI=20V～50V*	1,2,3	–	5.0	A
3	Output Ripple Voltage (Peak-to-Peak)	*VR*	BW=10kHz～6MHz, IO=5A	1	–	100	mV
				2,3	–	120	
4	Voltage Regulation	*SV*	*VI=20V→50V, IO=5A*	1,2,3	–	50	mV
5	Load Regulation	*SI*	*IO=0→5A*	1,2,3	–	50	mV
6	Input current	*IIN*	Full load, disable terminal 1 from connecting to input ground	1,2,3	–	14	mA
			Full load, disable terminal 2 to output ground		–	90	
			No load, no open end		–	100	
7	Input Reflected Ripple Current (Peak-to-Peak)	*IRIP*	BW = 20MHz, IO = 5A, connected to EMI filter	1	–	80	mA
				2,3	–	100	
8	Input Reflected Ripple Voltage (Peak-to-Peak)	*VRIP*	BW = 20MHz, IO = 5A, connected to EMI filter	1,2,3	—	500	mV
9	Switching frequency B	*fs*	*VI＝28V, IO=5A*	4,5,6	350	500	kHz
10	Efficiency	η	Input Voltage VI = 28V: IO = 5A	1	81	–	%
				2,3	79	–	

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			Input Voltage VI = 42V: IO = 5A	1	79	–	
				2, 3	77	–	
11	Short Circuit Power Consumption	*PD*	*VI = 28V, output short*	1, 2, 3	–	22	W
			VI = 42V, output shorted	1, 2, 3		24	
12	Capacitive load ab	*CL*	*VI = 28V, no effect on DC steady-state parameters*	4	–	1000	μF
13	Insulation resistance	*RISO*	Add 500V between input and output, and between any output terminal and case	1	100	–	MΩ
14	Output voltage change BC (peak) at load transition	*VLOR*	50% load → full or full load → 50% load, 10% load → 50% load or 50% load → 10% load	4	-600	600	mV
15	Recovery time of output voltage at load transition BCD	*tLOR*	50% load → full or full load → 50% load, 10% load → 50% load or 50% load → 10% load	4	–	600	μs
16	Output voltage change (peak) on input voltage jump be	*VVOR*	Input Voltage VI: 20V → 50V, IO = 5A Input Voltage VI: 50V → 20V, IO = 5A	4	-900	900	mV
17	Output voltage recovery time bde when input voltage transitions	*tVOR*	Input Voltage VI: 20V → 50V, IO = 5A Input Voltage VI: 50V → 20V, IO = 5A	4	–	600	μs
18	Starting overshoot B (peak)	*VTO*	Input Voltage VI: 0 → 28V, IO = 5A	4, 5, 6	–	50	mV
			Input Voltage VI: 0 → 42V, IO = 5A	4, 5, 6	–	50	mV
19	Startup delayf	*tTR*	Input Voltage VI: 0 → 28V, IO = 5A	4, 5, 6	–	10	ms

			Input Voltage VI: 0 → 42V, IO = 5A	4,5,6	-	10	ms
20	Load failure recovery time BD	*tLF*	*IO shorted to 5A*	4	-	10	ms
21	Forbidden Open Circuit Voltage	*VINH*	Open side prohibited, IO = 5A	1	-	16	V
22	Protective Power	*PW*	*IO≥6A*	1	72	-	W
23	External Synchronous Frequency Range B	*fSYNC*	*IO = 5A, 6 pins connected to TTL level (VIH ≥ 4.5V, VIL ≤ 0.8V), duty cycle 40% ~ 60%.*	4	400	500	kHz

A Capacitive load does not affect the DC parameters;

B This parameter is guaranteed by the design and is only tested during qualification inspections and design or process changes;

C. The transition time of the load should be greater than 10 μ s;

D The recovery time is the time from the start of the transition until the output voltage returns to within ± 1% of the corresponding stable value;

E The transition time of the input voltage shall be greater than 200 μs;

F The start-up delay time can be calculated either from the transition of the power supply or from the disconnection of the grounded forbidden terminal.

For the electrical parameters with change range requirements, the allowable change range is shown in Table 2.

Table 2 Allowable variation range of electrical parameters

Specific Property	Symbol	Condition (CL = 0 TC = 25 ℃, VI = 28V ± 0.5V, no open ends unless otherwise specified)	Electrical Parameter Allowance Rate of change	Unit
Output Voltage	$\triangle VO$	Full Load	±1	%
Efficiency	$\triangle \eta$	Full Load	±2	%

2.4 Electrical testing requirements

The electrical test requirements for the device shall be the relevant groups as specified in Table 3, and the tests for each group shall be as specified in Table 1 of this specification.

Table 3 Electrical Test Requirements

Project	Grouping
Intermediate Electrical Test (pre-conditioning)	A1、A4
Final electrical test (after conditioning)	A1a、A2、A3、A4 、A5、A6
Group a test requirements	A1、A2、A3、A4、A5、A6
Terminal electrical test group C	A1
Group E end point electrical test	Table 12
This group calculates the PDA.	

2.5 Electrostatic Discharge Sensitivity (ESDS)

The static level is grade 2, and the requirement is not less than 2000V.

2.6 Radiation Performance

The steady-state total dose shall not be less than 1000 Gy (Si) (R level) and 500 Gy (Si) (L level), and the single particle (burnout) shall not be less than 75 Mev. Cm2/mg (not less than 65 Mev. Cm2/mg according to the domestic actual particle level assessment).

2.7 Device Marking

2.7.1 Marking

a) Device identification number;

b) Positioning point;

c) Batch Identification Code or Date Code;

d) Name or trademark of the manufacturer;

e) Serial number;

f) Electrostatic Discharge Susceptibility (ESDS) identification number.

HDCD/ (20-50) -12-60/SP Mb C R/L

Device type package form lead plating RHA grade(R:TID≥1000Gy(Si)

L:TID≥500Gy(Si)

In addition, each device should be marked with a unique serial number continuously given, and should be marked with an identification code that can identify the sealing circumference, and the equilateral triangle (Δ) can be used as the mark of the electrostatic sensitive device, and can also be used as the identification mark of the first lead end.

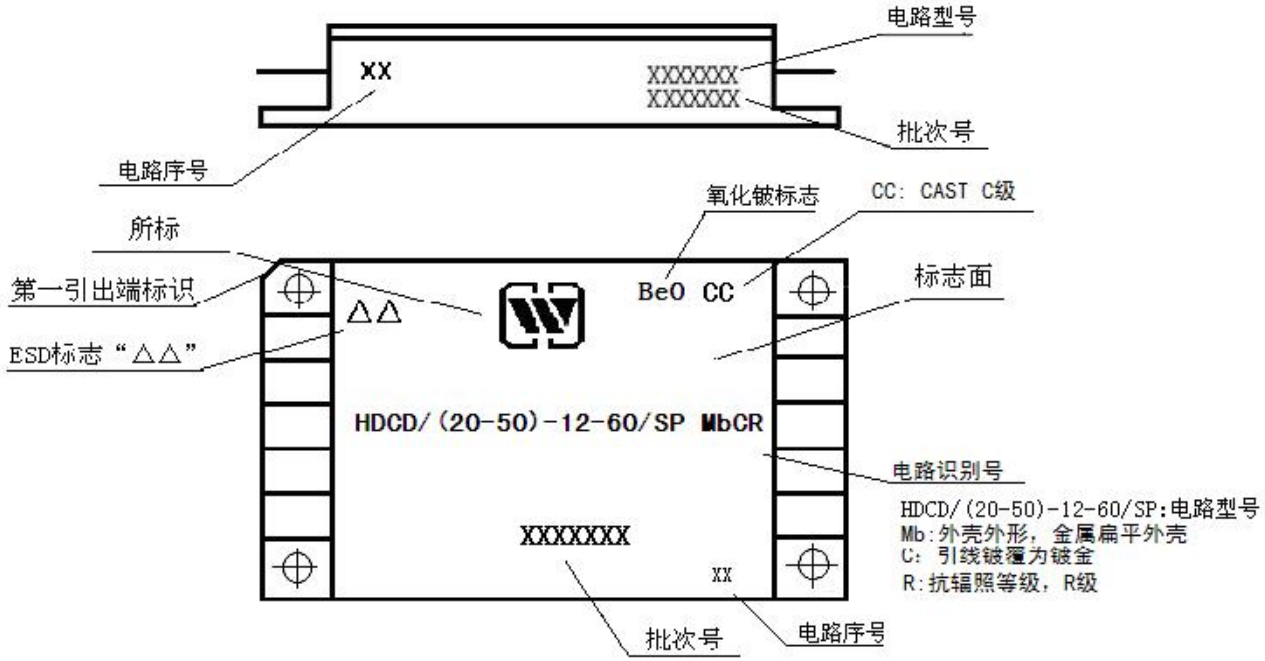
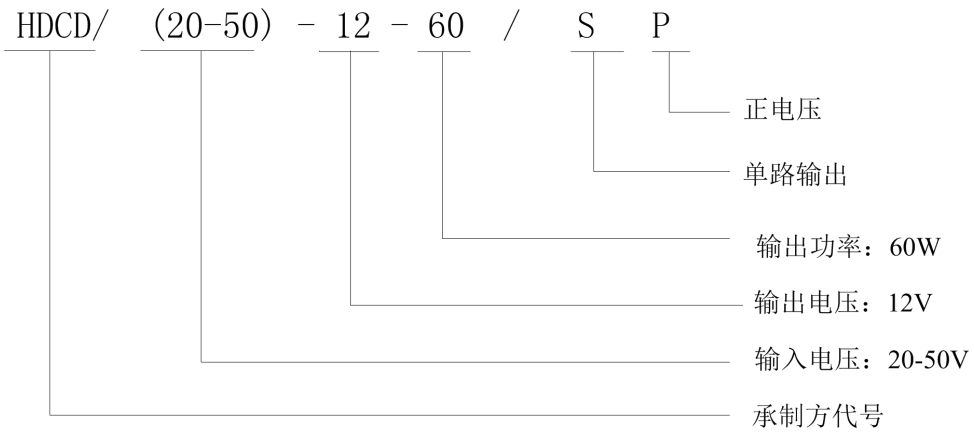


Fig. 4 Marking Diagram

2.7.2 Circuit type



2.8 Contractor outsourcing control

The process of device production and quality assurance should be completed by the device manufacturer. If outsourcing is required for some projects, the device manufacturer shall establish a management system for qualified outsourcing units, review the qualifications of the outsourcing units, and form a list of qualified outsourcing units. In case of any change in the

external cooperation unit of the YC class device manufacturer, the certification body and the user shall be notified.

2.9 Control Requirements for Purchased Raw Materials

2.9.1 General

The contractor shall confirm the production and appraisal qualification of the manufacturer of the purchased raw materials. Outsourced raw materials include at least substrates, bonding materials, bonding wires, enclosures, internal components, etc.

The Contractor shall prepare inspection documents for incoming materials purchased from outside, which shall specify the inspection method, sampling and inspection procedures, acceptance and rejection criteria and the test implementation period.

2.9.2 Changes in the state of raw materials

In case of any change in the state of the raw materials, the contractor shall notify the appraisal body (if required) and the user in written form of the relevant information on the state change within 5 working days.

3 Quality Assurance Provisions

3.1 Test classification

The inspection categories specified in this specification are as follows:

(A) Selection of the contractor;

(B) Identification tests;

C) Quality Consistency Inspection;

3.2 Selection of Contractors

Unless otherwise specified, all devices shall be screened as specified in Table 6 of this specification prior to qualification and quality conformance.

Table 6 Screening

Serial Number	Project	GJB 548B -2005		Request
		Method	Condition	
1	Internal visual inspectiona	2017.1	Condition K level	100%
2	Baking Stability	1008.1	150 deg C, at least 24 H or 125 deg C, at least 168 H	100%
3b	Temperature Cycle	1010.1	Condition C, 10 times	100%
4 b	Constant acceleration	2001.1	Direction Y1, 19600 M/S2	100%
5	Particle impact noise detection (PIND)	2020.1	Condition a	100%
6	Preconditioning electrical testc	—	As specified in Table 3 of this detail specification	100%
7	Aging	1015.1	*TC = 125 ℃, Test Scheme and Circuit Diagram of Aging Test* See figure 5, 240h	100%
8	Electrical test after conditioning	—	As specified in Table 3 of this detail specification	100%

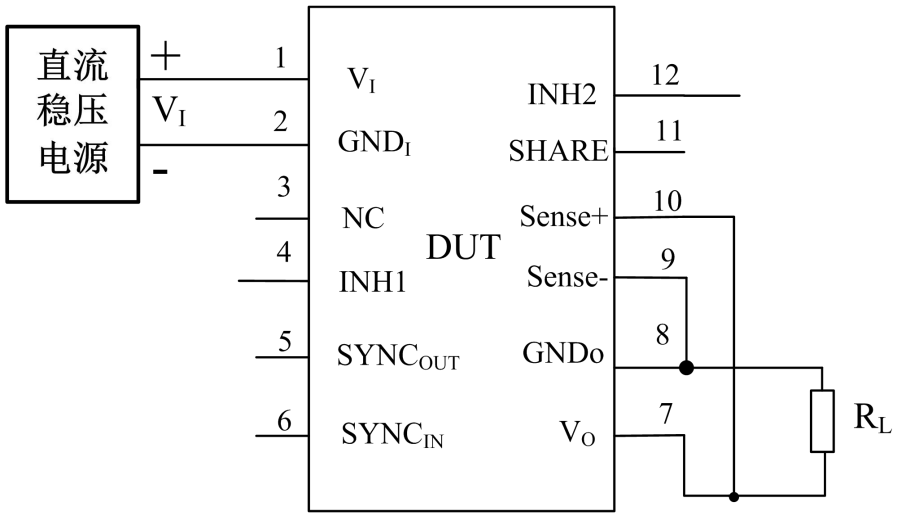
9	Calculate the variation and the rate of unqualified products.	—	As specified in Table 2 of this detail specification	100%
10	Allowable nonconformity rate (PDA) d	—	—	8% or 1 (whichever is greater)
11	Consistency of three temperature parameters in batch	—	Output voltage, efficiency, no-load current	± 3 σ, the parameter is provided as a reference, not as a criterion, only when the goods are supplied.
12	Sealing (fine and coarse leak detection)	1014.2	Fine leak detection: A1, pressure: 310kPa, time: 10h, R1 ≤ 5 × 10-3 (Pa.cm3)/s (He); Coarse leak detection: C1	100%
13	X-ray radiography	2012. 1	—	100%
14	External Visual Inspection	2009.1	—	100%

Circuits awaiting visual inspection before sealing should be stored in a dry, controlled environment.

After screening in group 3 and group 4, the manufacturer shall conduct external visual inspection of the circuit in accordance with GJB 548B-2005 method 2009.1.

The electrical test before the ageing test can eliminate circuits with unqualified electrical parameters, but the number of rejected products is not included in the rate of defective products; this test may not include all circuit parameters, but should include those that are most sensitive and effective in removing defective circuits Circuit parameters.

A typical failure is the failure of multiple circuits with the same root cause in an aged batch. PDA and typical failures only consider the static test data (group A1) of the circuit at 25 ° C. Functional failure does not exceed 5%.



Note: VI = 28V ± 3.0V, RL = 2.4Ω ± 10%/ (≥ 70W) or load current = 5A ± 10%.

Fig. 5 Block diagram of aging and steady-state life test

3.3 Identification

Qualification inspection shall be as specified in this specification, and the inspection carried out shall conform to the requirements of Group A, Group B, Group C, Group D and Group E of this specification, and the number of samples in Group C2 shall be 22 (0).

3.4 Quality Consistency Inspection (QCI)

The quality consistency inspection shall be in accordance with the provisions of this specification. The inspection shall be carried out in accordance with the provisions of Group A, Group B, Group C, Group D and Group E of this specification.

3.4.1 Group A test

Group a inspection shall be performed as specified in 4.8.3.1 of Q/QJA 20085-2012 and Table 7 of this specification.

Table 7 Group A test

Grouping	Pilot Project	n(0)
A1	Static test at 25 ℃	116(0)

A2	Static test at maximum rated operating temperature	76(0)
A3	Static testing at the lowest rated operating temperature	45(0)
A4	Dynamic test at 25 ℃	116(0)
A5	Dynamic testing at maximum rated operating temperature	76(0)
A6	Dynamic testing at the lowest rated operating temperature	45(0)
Note: Samples for Group A inspection shall be the circuit after screening. When the required sample size exceeds the batch size, 100% inspection is permitted. After the detection of the A1 group is completed, the other groups of the A group can be detected in an arbitrary order.		

3.4.2 Group B tests

Group B inspection shall be as specified in Table 8 of these Specifications.

Table 8 Group B test

Grouping	Pilot Project	GJB548B-2005 method	Test Condition	Sample size (number of allowable nonconformities) n (C)
B1	Physical size and weight	2016 and this specification 3.4	-	2(0)
B2	Particle impact noise detection (PIND) a	2020.1	Condition a	15(0)
B3	Solubility Resistance	2015	-	3 (0), laser marking not applicable

B4	Internal visual and mechanical inspectionb	2014	–	1(0)
B5	Bonding Strength	2011	–	2 (0), key joint wire is 22 (0), insufficient time is all
B6	Chip Shear Strength	2019	–	2 (0), according to the number of components is 22 (0), if insufficient, it is all
B7 c	Solderability	2003	–	1 (0), 15 leads (all if insufficient)
B8 d	Sealing Fine Leak Detection Rough leak detection	1014	Same as Table 6 of this specification	15(0)
B9 e	ESD A1	3015	ESD A. Electrical parameters, subgroup A1 b. ESDS 2000V C. Subgroup A1 for electrical parameters	3(0)
B10 e	Thermal Property	1012	Input voltage 28V, full load, heat sink, TC = 60 ℃,	3(0)

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			VDMOS and Schottky diode junction temperature not exceeding 100 ℃	
If 100% of the screening tests are performed with PIND, this test may not be performed. Internal visual inspection and structural inspection shall prove that the structure of the actual circuit meets the requirements of the archived design documents. Nickel-plated leads are pre-tinned. If the seal screening test is performed 100% between the final electrical test and external visual inspection, this item may not be performed. Appraisal or product technology, design changes.				

3.4.3 Group C tests

Group C inspection shall be as specified in Table 9 of these Specifications.

Table 9 Group C Test

Grouping	Test	GJB 548B-2005		Sample size
		Method	Condition	

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			QCI	Identification Test	(Number received)
C1	Resistance to welding heat	GJB 360B-210 in 2009	Condition a	Condition a	5 (0)
	External Visual Inspection	2009.1	-	-	
	PINDa	2020.1	Condition A, 5 yeses	Condition A, 5 yeses	
	Temperature cycleb Or Thermal Shock	1010.1	At least condition C, 20 cycles Or At least condition a	C. 100 cycles Not Applicable	
	Mechanical shockc And Constant acceleration	2001.1	Not Applicable 29400m/S2, direction Y1	Direction B, Y1 And 49000m/S2, direction Y1	
	Sweep vibration	2007	Condition a	Condition a	
	Sealing	1014.2	Same as Table 6 of this specification	Same as Table 6 of this specification	
	PIND	2020.1	Condition A, 1 pass	Condition A, 1 pass	
	Visual Inspection	1010.1	See Method 1010.1 in 3.2.	See Method 1010.1 in 3.2.	

	End Point Electrical Test		See Table 1 and Table 3 of this specification	See Table 1 and Table 3 of this specification	
C2	Steady Life	1005.1	*TC = 125 ℃, 1000h (see Figure 5 of this specification for the steady-state life test circuit diagram)*	*TC = 125 ℃, 1000h (see Figure 5 of this specification for the steady-state life test circuit diagram)*	22 (0) Or 8 (0) d
	End Point Electrical Test		See Table 1, Table 2 and Table 3 of this specification	See Table 1, Table 2 and Table 3 of this specification	
C3	Internal atmosphere content	1018.1	At 100 ℃ Water vapor content not more than 5000 ppm	At 100 ℃ Water vapor content not more than 5000 ppm	3(0)
C4	Internal visual inspection and structural inspection	2014	–	–	2(0)
	Wire Bonding Strength E	2011.1	–	–	
	Chip shear strength or Chip Bond Strength F	2019.2 2027.1	–	–	
C5	Thermal Vacuum Test	GJB1027A	*TC: -35 ℃ ~ 70 ℃, component appraisal level*	*TC: -35 ℃ ~ 70 ℃, component appraisal grade, see Appendix B*	5(0)

A PIND failure analysis shall be performed when the PIND test identifies a movable remainder within the circuit, provided that the Contractor can demonstrate that the remainder is controllable after corrective action has been taken and that the PIND test was performed in a random sample from a circuit manufactured using the baseline process.

B Thermal shock is not a substitute for temperature cycling for circuit qualification.

C Constant acceleration is not a substitute for mechanical shock for circuit evaluation. With the consent of the user, the values of constant acceleration and mechanical shock can be selected according to the package perimeter in accordance with Note d of Table 4 of the General Specifications.

D QCI inspection may be performed according to an 8 (0) sampling plan when all of the following requirements are met:

-- a maximum of 100 circuits per order;

-a maximum of 500 circuits may be ordered in a given equipment procurement contract;

-- Order up to a maximum of 500 circuits in a 12-month period.

E Test at least 2 circuits with a sample size (number received) of 15 leads (0).

F Shear tests shall be performed on all bonded chips and chip components in the circuit.

3.4.4 Group D test

Group D inspection The Group D inspection may be performed using sealed, empty enclosures that have been subjected to screening and stress conditions as specified in Table 10 of this

specification. Group D inspections are performed on the first inspection lot submitted for inspection, and subsequent inspection lots are redone at intervals of not more than 26 weeks.

Table 10 Group D test

Grouping	Pilot Project	GJB548B-2005 method	Test conditions of GJB548B-2005	Sample size (Number received)
D1	Thermal Shock	1011	C	5(0)
	Baking Stability	1008	150℃, 1h	5(0)
	Lead fastness	6.3.5 in 2004	B1	1(0)
	Sealing a. Fine Leak Detection b. Rough leak detection	1014	Same as Table 6 of this specification	5(0)
D3a	Salt fog	1009	A	5(0)
D4	Metal case insulation	1003	500V, 80nA Max	3(0)
The shell and cover can be inspected separately and the same type of tube and shell can be tested.				

3.4.5 Group E test

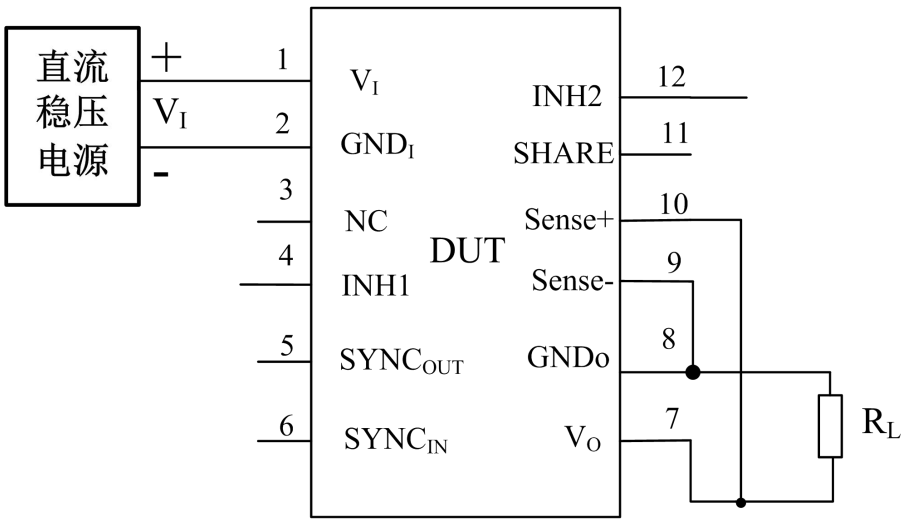
Group E shall be inspected as specified in Table 11 of this specification.

Table 11 Group E test

Subgroupsa	Test	Method	Condition and criterion	Sample size (number received)
E2a	Steady-state total dose irradiation	Q/QJA 20005-2012	R grade not less than 1000Gy (Si)(L level not less than 500 Gy (Si), dose rate 0.001 Gy (Si)/s, radiation test diagram and bias conditions see Figure 6.	4 (0)
	End Point Electrical Test		See table 12	
E5 b	Single Event Effect	Q/QJA 20008-2012	Maximum fluence rate: 10000ions/cm2 · s, LET ≥ 75 MeV · cm2/mg (65 MeV · cm2/mg). The unqualified criterion of single event transient effect is that the amplitude of transient waveform is relatively stable, the amplitude change of transient waveform is more than or equal to ± 10% of output voltage, and the minimum width of pulse width is more than or equal to 5ms, and the two conditions are satisfied at the same time. See Figure 6 for the radiation test plot and bias conditions.	3 (0)

Among them, 2 devices are biased, 2 devices are unbiased and all pins are short-circuited, and another device of the same model and specification is not irradiated for comparison test.

When specified in procurement documents or contracts, or during identification and design or process changes that may affect single-particle effects.



Note 1 For total dose test: test bias conditions VI = 50V ± 0.5V, RL = 4.8Ω ± 10%/ (≥ 40W) or load current = 2.5A ± 10%;

Note 2 For single event test: device 1 test bias VI = 20V ± 0.5V, RL = 4.8Ω ± 10%/ (≥ 40W) or load current = 2.5A ± 10%;

Device 2 test bias condition VI = 28V ± 0.5V, no load;

Device 3 Test bias conditions VI = 50V ± 0.5V, RL = 2.4Ω ± 10%/ (≥ 70W) or load current = 5A ± 10%.

Fig. 6 Radiation Test Circuit Diagram

Table 12 Group E Test Indicators

Specific Property	Symbol	Condition (TA = 25 ℃, VI = 28V ± 0.5V and VI = 42V ± 0.5V, forbidden open circuit, CL = 0, unless otherwise specified)	A-group Grouping	Extremely		Unit
				Minimal	Maximal	
Output Voltage	*VO*	*IO=5A*	1	11.43	12.69	V
Output Current	*IO*	*VI=20V～50V*	1	-	5000	mA

Output Ripple Voltage (Peak-to-Peak)	*VR*	BW=10kHz～6MHz, IO=5A	1	—	120	mV
Voltage Regulation	*SV*	*VI=20V→50V, IO=5A*	1	—	60	mV
Load Regulation	*SI*	*IO=0→5A*	1	-	60	mV
Input current	*IIN*	Full load, disable terminal 1 from connecting to input ground	1	—	17	mA
		Full load, disable terminal 2 to output ground			110	
		No load, no open end		—	150	
Input Reflected Ripple Current (Peak-to-Peak)	*IRIP*	BW=20MHz, IO=5A	1	—	100	mA
Input Reflected Ripple Voltage (Peak-to-Peak)	*VRIP*	BW=20MHz, IO=5A	1	—	500	mV
Efficiency	η	Input Voltage VI = 28V: IO = 5A	1	78	—	%
		Input Voltage VI = 42V: IO = 5A	1	76	—	
Short Circuit Power Consumption	*PD*	*VI = 28V, output short*	1	—	22	W
		VI = 42V, output shorted	1	-	24	
Insulation resistance	*RISO*	Add 500V between input and output, and between any output terminal and case	1	100	—	MΩ
Forbidden Open Circuit Voltage	*VINH*	Open side prohibited, IO = 5A	1	-	16	V
Protective Power	*PW*	*IO≥6A*	1	72	-	W

4 Preparation for delivery

The storage environment of packaged products shall meet the requirements of temperature: 15 ℃ ~ 25 ℃, humidity: 25% ~ 65%, no acid, alkali or other corrosive gases around, good

ventilation, and corresponding anti-static measures.

5 Explanatory remarks

5.1 Intended use

Devices conforming to this detail specification are intended for use in the aerospace field or in military equipment. In order to achieve the best cost performance while maintaining the basic quality and reliability requirements of the devices, the devices with appropriate grade and application should be purchased according to the actual needs.

5.2 Procurement document requirements

The following contents shall be specified in the procurement documents:

A) The number of the detail specification;

(B) The name of the product;

C) Quality Assurance Level;

(D) The quantity ordered;

E) Requirements for supervision and acceptance;

F) Special requirements of the user, such as requirements for radiation resistance, etc.

5.3 Application Notes

Use and operation of this circuit shall be in accordance with this specification and the application manual.

The use and operation of this circuit shall be in accordance with the functional wiring of each pin as shown in the pin function table to ensure the correctness of electrical connection, the effectiveness of anti-static measures and the effective grounding of the grounding terminal.

It is recommended to install on the heat dissipation bottom surface or side wall surface of user equipment structural parts and ensure good heat dissipation.

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